REMARKS

Claims 1 - 30 are pending in this application. Claims 1 - 30 have been subjected to a restriction requirement under 35 USC 121. Accordingly, the claims have been restricted to one of the following inventions:

I. Claims 1 - 9 and 19 - 21 drawn to a multilayer chip carrier, classified in class 174 subclass 260.

II. Claims 10 - 18 drawn to a multilayer chip carrier substrate, classified in Class 174 subclass 260.

III. Claims 22 - 30 drawn to a method of fanout redistribution of signal pads on multilayer chip carrier, classified in class 29 subclass 825.

The Examiner has stated that the product inventions of I and II are distinct from the method invention of III since the product can be made by another and materially different process. The Examiner goes on to state that, for example, the "product could be made by a method wherein the plurality of signal pads are not arranged adjacent a plurality of power distribution busses". However, it is not clear to Applicants how not carrying out a step acts to provide a materially different process.

Regardless, Applicants affirm the election made by their attorney (J.A. Jordan) on November 9, 2005. In accordance with that election, Applicants elected with traverse to prosecute the Invention of Group I directed to a multilayer chip carrier as set forth in Claims 1 - 9 and 19 - 21.

Accordingly Claims 10 - 18 and 22 - 30 have been withdrawn from further consideration by the Examiner as being drawn to a non-elected invention.

The specification at page 10 has been amended to correct the informality noted by the Examiner.

Claim 1 has been amended in accordance with the suggestion of the Examiner to provide proper antecedent basis. Accordingly, the objection to Claim 1 is overcome. Claim 19 has also been amended to correct a discrepancy in claim language.

Claims 11 - 18 have also been objected to because of discrepancies in claim language. Applicants agree, as confirmed by phone on November 9, 2005, that Claims 11 - 19 should be -- a multilayer chip substrate -- . However, in view of the Examiner's withdrawal of these claims from further consideration, Applicants believe that any amendment to these claims to eliminate any discrepancies, should be held in abeyance until these claims are under consideration.

The 35 USC 103(a) Claim Rejections on APA in View of Lin

Claims 1, 2, 8, 9 and 19 - 21 have been rejected under 35 USC 103(a) "as being obvious over Admitted by Applicant (Prior Art, hereinafter 'APA') in view of Lin (Patent # 5,258,648 hereinafter 'Lin'").

The Examiner states, in regard to Claim 1, that Claim 1 reads on the APA "except APA doesn't explicitly teach set of signal pads each having a conductive line connected thereto extending to connect to respective signal pads positioned nearer the said edge of said chip footprint". For this latter limitation, the Examiner relies upon Lin.

In relying on Lin, the Examiner asserts that "Lin discloses in Fig. 1 set of signal pads 24 each having a conductive line 26 connected thereto extending to connect to respective signal pads 27 positioned nearer the said edge of said chip footprint". The Examiner goes on to assert that it would have been obvious, at the time the invention was made, for APA to include "that set of signal pads each having a conductive line connected thereto extending to connect to respective signal pads positioned nearer the said edge of said chip footprint to provide options for signal contact escape".

The Lin Patent

The Lin patent is directed to a composite flip chip semiconductor device having a single semiconductor die and having an integrated circuit formed thereon and a plurality of bonding pads electrically coupled to the integrated circuit. The device further includes an interposer having first and second surfaces and a plurality of vias extending from the first surface to the second surface. The first surface of the interposer has a plurality of conductive traces which are electrically coupled to the plurality of vias. Means for electrically coupling the plurality of bonding pads to the plurality of traces are included in the device as well as means for electrically coupling the plurality of vias to a substrate.

Thus, Lin describes an interposer arrangement having some pads 27 lining up with some of solder bumps 16 on chip 12 with such signal pads having line traces 26 extending inwardly from the edge of the chip footprint. The inwardly extending line traces 26 appear to directly connect to electrical vias 24. Although the Examiner states that "via 24 have to have pads" (emphasis added), Applicants do not understand why such

would be the case. It would appear that, as shown in Lin, the line traces could connect directly to the electrical vias.

More significant, however, is the fact that conductive line traces are taught by Lin to "fan in". This can be seen by reference to Lin's statement in Column 5, lines 42 et seq. There, Lin states that "Fig. 5 demonstrates how conductive traces 26 can be used to 'fan in' peripheral solder bumps 16 to a predetermined via or solder ball configuration".

Contrary to Lin, Applicants' invention is directed to signal escape or "fanning out". Applicants' reference such, for example, on page 5 wherein Applicants state "layer 3, shown as FC3, acts as the first fanout signal redistribution layer from the chip, and layer 21, shown as FC1, acts as the second fanout signal redistribution layer from the chip".

Accordingly, Lin's teachings run counter to the so called APA relied upon by the Examiner. Given these contrary teachings, it is not at all clear to Applicants how one skilled in the art would want to combine Lin with the APA, as relied upon by the Examiner.

For example, Lin teaches nothing about signal escape methods and structure in a multilayer chip carrier. Lin is directed to solving problems, such as, burning-in and rework of flip chip devices. Lin solves these problems by providing a particular interposer structure that allows burn-in and rework of flip chips. To achieve this, Lin's structure is such that signals originate from the chip solder balls 14 and conduct from pads 27 inwardly from the chip footprint edge to vias 26. Applicants' signals, on the other hand, originate from chip solder balls and conduct outwardly to the chip footprint edge. Given the disparate teaching of Lin and the APA, it is not at all clear why one

skilled in the art would be motivated to combine Lin with the APA. Accordingly, Applicants believe that the Examiner has failed to make out a case for prima facia obviousness.

Although it is not clear why one skilled in the art would be motivated to combine Lin with APA, even when combined the combination fails to anticipate Applicants' claimed invention. For example, Claim 1 recites "a layer of dielectric material having a plurality of signal pads formed thereon in a pattern of signal pads related to a pattern of signal pads within the footprint of at least one chip to be carried on said chip carrier" (emphasis added). Thus, the recited signal pads on the layer of dielectric material obtain their signals from the chip.

Claim 1 goes on to recite "said plurality of signal pads including a first set of signal pads near the edge of said chip footprint each having a conductive line extending beyond the edge of said chip footprint and a second set of signal pads each having a conductive line connected thereto extending to connect to respective signal pads positioned nearer the said edge of said chip footprint".

The combination of references relied upon by the Examiner does not teach "a second set of signal pads each having a conductive line connected thereto extending to connect to respective signal pads positioned nearer the said edge of said chip footprint". The signal pads of Lin are pads 27 as determined by signals coming from the chip 12 solder balls. The signal pads extend inwardly to vias 24. Thus, Lin does not teach "signal pads each having a conductive line connected thereto extending to connect to respective signal pads positioned nearer the said edge of said chip footprint" (emphasis added).

Thus, the claimed limitations calling for the escape of signal pads near the edge of the chip footprint and the extending or moving of non-escaping signal pads nearer the edge of said chip footprint is not taught by the combined references, even if it were proper to so combine. Again, given the differences between Lin and the APA, there is clearly nothing to suggest or teach combining these references. It appears, in this regard, that the Examiner is using Applicants' teachings in an effort to construct a device to meet Applicants' claimed invention. Clearly, Applicants' teachings of moving non-escaping signal pads closer to the chip edge at the same time or level that other signal pads escape, so as to provide additional space for PTHs, is not taught by the art relied upon by the Examiner.

The Examiner's rejection of Claims 2, 8 and 9 on APA and Lin also fails to make a prima facia case of obviousness for the same reasons the rejection of Claim 1 on APA and Lin fails to make out a case of prima facia obviousness. In addition, Claim 2 recites additional limitations not found in the art relied upon.

For example, as recited in Claim 2, Lin fails to show "at least some of said signal pads ... near the edge of said chip footprint having a conductive via connected thereto". In the rejection of Claim 1, the Examiner has read the signal pads in question, i.e., "nearer the said edge", on pads 27 of Lin. Now, in rejecting Claim 2, the Examiner is reading these same pads on solder balls 14 and the Claim 2 recited conductive vias on vias 24 of Lin. Such an interpretation is inconsistent with and undermines the Examiner's interpretation of Lin in the original rejection of Claim 1 from which Claim 2 stems. How can this be?

In rejecting Claim 19 on the APA and Lin, the Examiner continues an erroneous and unclear interpretation of Lin. If the second recited "signal pads" is to be read on vias 24 of Lin, the recited "conductive lines" on lines 26 of Lin and the recited "signal pads positioned closer to the edge of said chip footprint" on pads 27, then where are the recited "conductive vias" connected to the latter? Applicants do not understand the Examiner's explanation of the interpretation given in this rejection. How do solder bumps 14 work into this interpretation? They are connected to vias 24 but don't meet the previously by recited limitations of the claim.

Claim 19 further recites "a second layer of dielectric material having a set of signal pads ... connected to said conductive vias extending through said first layer of dielectric material and having respective conductive lines connected thereto extending to respectively connect to further signal pads positioned closer to the edge of said chip footprint" with "said further signal pads having conductive vias connected thereto extending through said second layer of dielectric material".

The Examiner apparently reads the limitations in this second paragraph on APA and Lin in the same erroneous manner as provided in regard to the first paragraph of Claim 19. In addition, the Examiner further dismisses this paragraph as a "mere duplication of parts". However, the various claim limitations of paragraphs 1 and 2 are more than mere parts but rather are novel structure designed to provide more space for PTHs, and using two layers or steps to move the signal pads closer to the edge before escape gives even more additional space for the PTHs. The combination of the APA and Lin cannot reasonably be interpreted to do this.

The third paragraph of Claim 19 calls for escape of the signal pads. Again, the APA and Lin cannot reasonably be interpreted to meet the limitations of this paragraph. Clearly, there is nothing in Lin to teach or suggest using two steps to move signal pads closer to a chip edge and then move the signal pads to escape the chip.

Accordingly, the rejection of Claim 19 is improper for the same reasons as the rejection of Claim 1 and for the additional reasons set forth in regard to the additional limitations of this claim.

Again, Applicants firmly believe that one skilled in the art would not be motivated to combine Lin with the APA and, even when somehow combined, the combination fails to anticipate the various claim limitations of Claims 1, 2, 8, 9 and 19 - 21.

The 35 USC 103 Claim Rejections on APA in view of Lin and Arima, et al.

The Examiner has rejected Claims 3 - 7 under 35 USC 103(a) as being obvious over APA in view of Lin and in view of Arima, et al.

In regard to this rejection, the Examiner states that APA discloses "all of the claimed features, as discussed in the rejection of Claim 2, including a further layer of dielectric material beneath said layer of dielectric material having signal pads, 37 and 37A thereon (FC2 Layer, Fig. 5) ... except APA doesn't explicitly teach respective ones of said signal pads connected to respective ones of said conductive vias of said set of conductive vias". For this the Examiner apparently relies upon Arima, et al.

It is not clear to Applicants, however, why and how the Examiner is relying on Arima, et al. Regardless, this rejection fails for the same reasons the Claim 1 rejection

fails. Lin not only fails as a reference because it is not such that one skilled in the art would be motivated to combine it with APA, but also because, even if combined, it fails to meet the limitations of Claim 1. The vias in question in Claim 3 are vias connected to the claimed signal pads positioned near the edge of said footprint, for which the Examiner has previously relied upon Lin. However, again, Lin doesn't teach such structure, as hereinabove explained. Lin also does not teach the vias claimed in Claim 2. Lin also does not teach the further layer of dielectric material, set forth in Claim 3.

It is noted that the Examiner rejected Claims 19 - 21 on APA and Lin. It is also noted that some of the same limitations recited in Claim 19 are akin to the limitations recited in Claims 3 - 5 for which the Examiner is relying upon APA, Lin and Arima, et al. Arina, et al. merely teaches that vias may have pads connected at each end thereof. It is not clear how this teaching aids in the rejection of Claims 3 - 5. Regardless, Applicants have already clearly pointed out how Claim 19 distinguishes over APA and Lin and Arima, et al. doesn't add anything to rebut these distinctions.

Accordingly, the rejection of Claims 3 - 7 under 35 USC 103(a) as being obvious over APA in view of Lin and in further view of Arima, et al. is improper for the same reasons, as explained above, the rejection of Claims 1, 2, 8, 9 and 19 - 21 is improper.

Conclusion

In view of Applicants' amendment and remarks, Applicants firmly believe that the rejected claims are now clearly in condition for allowance. Accordingly, Applicants

respectfully request the Examiner to reconsider and withdraw the outstanding rejection, and allow the rejected claims as now presented.

Respectfully submitted,

Jean Audet, et al.

By: _____
John A. Jordan, Attorney
Registration No. 24,655
Tel. (518) 587-1902

WHS/JAJ